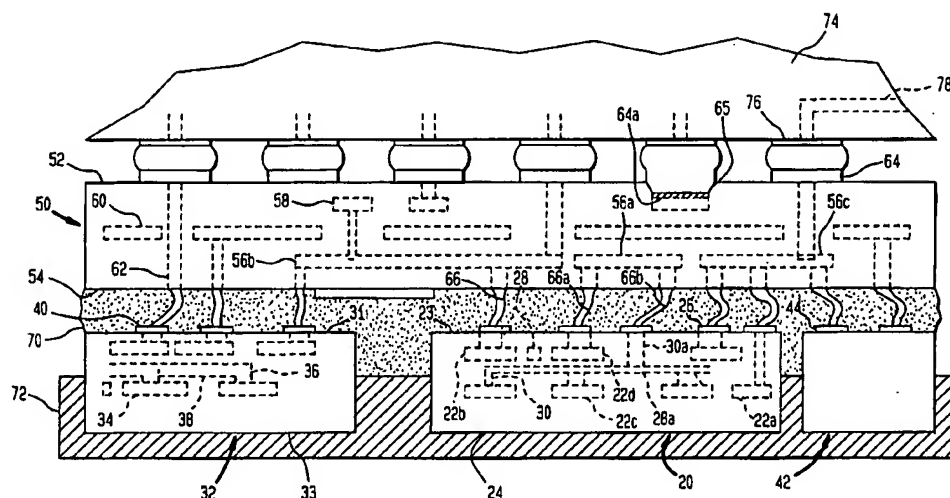




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(54) Title: CHIP WITH INTERNAL SIGNAL ROUTING IN EXTERNAL ELEMENT



(57) Abstract

A semiconductor chip (20) is provided with a dielectric element (50) having conductive features (56a) interconnecting electronic elements (22a, 22d) within the chip with one another. The conductive features replace internal conductors, and can provide enhanced signal propagation between elements of the chip. The conductive features on the dielectric element are connected to contacts on the chip by deformable conductive elements such as flexible leads (66) so that the dielectric element remains movable with respect to the chip. The dielectric element may have a coefficient of expansion different from that the chip itself.

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CHIP WITH INTERNAL SIGNAL ROUTING IN EXTERNAL ELEMENT
TECHNICAL FIELD

The present invention relates to semiconductor chips.

5 BACKGROUND ART

Semiconductor chips commonly incorporate myriad electronic elements such as transistors, capacitors, resistors and the like, together with more complex electronic elements such as logic gates, amplifiers, comparators, and many other passive and active electrical components. These elements typically are provided in one or more layers extending parallel to the front and back surfaces of the chip. The various electronic elements of the chip typically are interconnected with one another by metallic traces extending within the chip in the horizontal or "X" and "Y" directions and metallic vias extending in the vertical or "Z" direction. Typically, the traces and vias are formed of conductive material deposited during fabrication of the chip as, for example, aluminum or polysilicon. The traces and vias used to interconnect the electronic elements of the chip with one another complicate design and fabrication of the chip.

Moreover, the traces which are fabricated during manufacture of the chip do not always provide optimum electrical characteristics. For example, the traces typically are formed from aluminum, which has a relatively high resistivity. Although processes for fabricating traces in a chip from low-resistivity metals such as copper are known, these processes impose special requirements in chip fabrication. Further, even if a low-resistivity metal is employed, the size and hence the cross-sectional area of traces which can be accommodated within a chip are subject to severe limitations. Traces extending within a chip often follow indirect routes because other elements of the chip lie in a direct route between the electronic elements connected by the trace.

30 Additionally, chips must be connected to external circuit elements. In the conventional approach to chip packaging, each chip is

incorporated in a separate package bearing leads or other external connecting elements. Contacts on the surface of the chip are connected to these external connecting elements. The external connecting elements on the package are connected to a conventional circuit board or other circuit-bearing substrate.

5 Alternatively, several chips may be mounted in a single package, commonly referred to as a "multichip module." These chips may be connected to one another and to a common set of external connecting elements, so that the entire assembly can be mounted to the substrate as a unit. In yet another alternative, the chip itself is attached directly to the substrate.

10 As described in Arima et al., United States Patent 5,281,151, a package in the form of a rigid ceramic board may be provided with a set of "thin film" circuit layers overlying the ceramic board. The thin film layers include metallic traces on a material such as polyimide which has a relatively low dielectric constant. A chip is mounted to the thin film layers by solder
15 balls in engagement with contacts on the chip. A signal can be routed from point to point within the chip along a signal path through a solder ball at one location on the chip, along a metallic trace of the thin film element and back into the chip through a solder ball at another location on the chip. The thin film layer assertedly provides low resistance and relatively rapid signal
20 transmission between elements of the chip.

As described in commonly assigned U.S. Patents 5,148,265; 5,148,266; 5,455,390, 5,518,964, 5,688,716 and International Publications WO 96/02068 and WO 97/11486, the disclosures of which are all
25 incorporated by reference herein, it is desirable to provide interconnections between the contacts on a chip and external circuitry by providing a further dielectric element, which may be referred to as a "interposer" or "chip carrier" having terminals. Terminals on the dielectric element are connected to the contacts on the chip by flexible leads. The terminals on the dielectric element may be connected to the substrate as, for example, by solder bonding the
30 terminals to contact pads of the substrate. The dielectric element remains

including a first semiconductor chip 20 having a front surface 22 and numerous internal electronic elements 22 so that upon reviewing the specification, one immediately realizes that numeral 22 could not have been intended to refer to both elements. Thus, the replacement pages replace numeral 22 with numeral 23 at page 10, line 24, page 11, lines 7, 10, and at page 12, line 3. A set of formal drawings incorporating this change is submitted herewith.

In addition, it is immediately apparent that "chips 28 and 32" could not have been intended at page 12, line 2 because throughout the specification, the first semiconductor chip is assigned reference numeral 20 and the second semiconductor chip is assigned reference numeral 32, whereas reference numeral 28 throughout the specification denotes internal conductive traces of chip 20. Fig. 1 clearly shows reference numeral 28 indicating a trace within chip 20 and reference numeral 20 indicates the chip having electronic elements 22 included therein. This error is immediately apparent because throughout the specification reference numeral 20 refers to the chip whereas reference numeral 28 refers to traces within the chip. Thus, replacement page 12 correctly uses reference numeral 20 to refer to the chip. Likewise, "multi-layer traces 58 and 56" could not be intended at page 13, line 10. On page 12, line 7 the specification indicates: "The dielectric element further includes substantially continuous electrically conductive potential reference plane elements 60. Only a few traces 56 and 58 dispersed in two layers are depicted in Fig. 1". The error on page 13 is immediately apparent because page 12 clearly indicates that reference numerals 58 and 56 are assigned to the multi-layered traces. Thus, replacement page 13, at

lines 10 and 14, correctly uses reference numeral 56 to refer to the multi-layer trace.

"Dielectric element 150 includes internal potential reference planes 160 and traces 150" could not have been intended at page 15, line 30 through page 16, line 1 because the dielectric element and the traces are clearly separate elements which cannot each have reference numeral 150 assigned to them. In addition, reference numeral 150, throughout the specification, is assigned to the dielectric element. As clearly indicated in Fig. 2, reference numeral 156 indicates traces within the dielectric element 150. It is also immediately apparent that "potential plane 294" could not have been intended at page 24, line 30. The specification indicates at page 25, lines 4-5 "transmission line 290 branches to form two further transmission lines 294 and 295." Thus, reference numeral 294 could not refer to the separate elements of the potential plane and the branch transmission line. Furthermore, reference numeral 294 is used throughout the specification to refer to the branch transmission line. Thus, replacement pages 24 and 25 are provided to use reference numeral 291 to refer to the potential plane. A set of formal drawings incorporating this change is submitted herewith. In addition, replacement page 25 is provided to use reference numeral 298 to indicate the terminal 298 shown in Fig. 8.

Replacement page 32 corrects typographical errors at lines 26-27. Lines 25-26 provides: "The distal end of the second conductor terminates proximally of via 953 and mask 969", however, throughout the specification "mass 969" is used. It is therefore obvious that on line 26 "mask" is a typographical error. Furthermore, lines 26-27 at page 33 indicates "the first

elements and the interconnect traces on the dielectric element. Preferably, a compliant material is provided between the chip and the dielectric element to provide mechanical decoupling between the chip and the dielectric element.

5 In the preferred assemblies according to this aspect of the invention, signals travel between electronic elements of a single chip through the traces on a separate dielectric element which remains movable with respect to the chip. The dielectric element can have a coefficient of thermal expansion different from that of the chip. The deformable conductive elements will compensate for movement of the traces relative to the contacts
10 on the chip. The ability to use a dielectric element having a coefficient of expansion different from that of the chip allows the designer to use dielectric layers such as polyimide layers with substantial copper features. Structures of this type have electrical properties such as high conductivity and relatively low dielectric constant, but have thermal expansion properties close to those
15 of copper and significantly different from those of the chip.

The dielectric element may be a flat element such as a platelike or sheetlike element having a bottom surface and a top surface opposite from the bottom surface. Most preferably, the dielectric element includes a flexible polymeric sheet or a laminate including plural sheets, having one or more
20 layers of interconnect traces thereon. Where the dielectric element is a flat plate or sheet, the interconnect traces generally will extend in horizontal directions, parallel to the top and bottom surfaces of the dielectric element.

According to a further aspect of the invention, a semiconductor chip assembly includes a first semiconductor chip as aforesaid and a dielectric
25 element separate from the chip. The dielectric element has a plurality of conductive features thereon. At least some of said contacts are connected with at least some of the conductive features so that at least some of the electronic elements of the chip are connected to one another by the conductive features. The conductive features on the dielectric element include at least
30 one set of plural conductive features defining a multiconductor transmission

line extending between spaced-apart locations on the dielectric element. The electronic elements of the chip include at least one pair of multiply-connected elements, each said pair of multiply-connected elements is connected to one another through the plural conductive features of one said transmission line.

5 For example, the conductive features of the dielectric element may include interconnect traces as aforesaid and conductive potential reference elements such as substantially continuous electrically-conductive potential planes. The interconnect traces may be arranged in layers so that some or all of the trace layers are juxtaposed with potential planes. Thus, the
10 traces in these layers are juxtaposed with the potential planes so that each trace and the adjacent potential plane forms a transmission line of the type commonly referred to as a stripline. In such an arrangement, one potential plane may serve as a part of several transmission lines. Alternatively or additionally, the conductive features on the dielectric element may include
15 sets of traces extending adjacent one another, such as two or three traces extending alongside one another. The traces of each such set may define a single multiconductor transmission line. The transmission line configurations discussed above minimize crosstalk between different signals and reduce susceptibility to electromagnetic interference. Further, the transmission lines
20 preferably provide controlled impedance along the length of the transmission line. Most preferably, the characteristic impedance of the transmission line does not change abruptly at any point along the length of the transmission line. Assemblies according to this aspect of the invention provide rapid propagation of signals between widely separated elements on the chip. The
25 most preferred assemblies take advantage of both aspects of the invention, and hence include multiconductor transmission lines on a dielectric element which is connected to the chip through deformable conductive elements and movable with respect to the chip.

 At least some ends of the transmission lines, the conductive
30 features of the transmission line are connected to a multiply-connected

element of the chip through a plurality of adjacent contacts on said chip. Ends where such connections are provided are referred to herein as "adjacent-connected" ends of the transmission lines. The deformable conductive elements may include flexible leads connecting the conductive features of each transmission line to the contacts on the chip at each such adjacent-connected end. The flexible leads at each adjacent-connected end may include plural separate flexible leads extending next to one another. The leads may be physically parallel to one another. Most preferably, the leads are curved in horizontal directions parallel to the surface of the chip, and the curved leads are nested within one another. The parallel leads provide an extension of the multiconductor transmission line. The parallel leads desirably provide a characteristic impedance close to the characteristic impedance of the transmission line itself.

Alternatively, the flexible leads at least some of said adjacent-connected ends may include a plural-conductor flexible lead incorporating a plurality of conductors extending next to one another and a dielectric between such conductors. Typically, a single plural-conductor lead provides the sole connection of the stripline to the contacts at an end of the transmission line. Here again, the plural-conductor lead can be impedance-matched to the transmission line.

Typically, the electronic elements of the chip are arranged to send and receive digital signals in synchronism with a common clock, such as the internal clock of the chip itself. As discussed below, the transmission lines provide rapid signal transmission between the elements and thus allow operation of the chip at a high clock speed. The transmission lines on the dielectric element may distribute the clock signal itself. The transmission lines may be provided in a branching pattern with characteristic impedances selected to suppress signal reflections at the branching points.

The dielectric element may be provided with terminals for connection to an external circuit or substrate. For example, the dielectric

element desirably overlies the front surface of the chip, so that a bottom surface of the dielectric element faces towards the front or contact-bearing surface of the chip. A compliant layer desirably is disposed between the dielectric element and the chip. Terminals on the dielectric element may be accessible at the top surface of the dielectric element, facing away from the chip. Thus, the terminals may project from the top surface or may be recessed within holes or vias extending into the dielectric element from the top surface. Some or all of the terminals on the dielectric element may be connected to the first chip through the deformable conductive elements, so that the first chip can be connected to an external substrate by connecting the terminals to contact pads on the substrate. In this instance, the dielectric element and deformable conductive elements serve as part of the package for the chip. The assembly may further include a second semiconductor chip having electronic elements therein. The second semiconductor chip also may be juxtaposed with the dielectric element and may be connected to at least some of the traces on the dielectric element. Thus, the traces on the dielectric element may also form interconnections between the first and second chips so as to provide a multichip module. The assembly may further include one or more auxiliary circuit elements such as capacitors or other discrete components juxtaposed with the dielectric element and connected to at least some of the traces. The traces connect the chip or chips to the auxiliary circuit element as well.

Still further aspects of the present invention provide methods of making semiconductor assemblies. Methods according to this aspect of the invention preferably include the step providing a unitary semiconductor structure having a front surface. The semiconductor structure may be a chip or wafer incorporating a plurality of electronic elements within said structure and contacts on the front surface. The electronic elements have signal connections and are adapted to send and receive time-varying signals through these connections. Preferably, the electronic elements also have constant-

potential connections such as ground and/or power connections. At least some of the signal connections are connected to the contacts. The method according to this aspect of the invention further includes the step of assembling a dielectric structure having electrically conductive features thereon to said semiconductor structure so as to connect the electrically conductive features with said contacts through deformable conductive elements. The assembling step is performed in such a manner that that signal connections of at least some of the electronic elements within said unitary semiconductor structure are connected to one another through the contacts, the deformable conductive elements and the conductive features on said dielectric structure. The assembling step is also performed in such a manner that the dielectric structure remains movable with respect to said semiconductor structure.

The unitary semiconductor structure may include a plurality of chips. In this case, the assembling step desirably is performed so that electronic elements within each said chip are connected to one another through conductive features within a portion of the dielectric structure associated with that chip. The method may further include the step of severing the unitary semiconductor structure to separate each said chip from the unitary semiconductor structure so that the portion of the dielectric structure associated with such chip remains with the chip.

Methods according to this aspect of the invention can be used to fabricate assemblies as discussed above.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a diagrammatic sectional elevation view depicting an assembly in accordance with one embodiment of the invention.

Fig. 2 is a diagrammatic perspective view depicting an assembly in accordance with another embodiment of the invention.

Fig. 3 is a fragmentary diagrammatic view depicting an assembly in accordance with another embodiment of the invention.

Fig. 4 is a fragmentary perspective view depicting an assembly in accordance with a further embodiment of the invention, with portions
5 removed for clarity of illustration.

Figs. 5 and 6 are views similar to Fig. 4 depicting assemblies according to other embodiments of the invention.

Fig. 7 is a fragmentary sectional view taken along line 7-7 in Fig. 6.

10 Fig. 8 is a view similar to Fig. 4 depicting an assembly according to yet another embodiment of the invention.

Fig. 9 is a diagrammatic plan view depicting an assembly in accordance with another embodiment of the invention.

15 Fig. 10 is a view similar to Fig. 1 but depicting an assembly in accordance with a further embodiment of the invention.

Fig. 11 is a fragmentary sectional view depicting a component in accordance with a further embodiment of the invention.

Fig. 12 is a fragmentary elevational view depicting an assembly incorporating the component of Fig. 11.

20 Figs. 13 and 14 are diagrammatic perspective views depicting steps in processes according to further embodiments of the invention.

MODES FOR CARRYING OUT THE INVENTION

The assembly includes a first semiconductor chip 20 having a front surface 23, a rear surface 24 and a plurality of contacts 26 on the front
25 surface. Chip 20 includes numerous internal electronic elements 22, of which only a few are depicted in Fig. 1. In actual practice, typical chips include hundreds of thousands or millions of such electronic elements. Electronic elements 22 may include conventional analog elements, digital

elements or both. Most commonly, the electronic elements are conventional digital circuit

elements such as logic gates, flip-flops, and registers. These may be clock-timed elements arranged to send and receive digital signals in synchronism with clock common to all of these elements as discussed below. The clock may be one of the electronic elements of the chip.

5 Electronic elements 22 are disposed in numerous layers, of which only two are depicted in Fig. 1, i.e., a bottom layer closer to bottom surface 24 and a top layer closer to front surface 23. The bottom layer includes element 22A, whereas the top layer includes element 22B. The chip further includes internal conductive traces 28 extending in horizontal
10 (X and Y) directions parallel to the front and back surfaces 23 and 24 of the chip as well as electrically conductive vias 30 extending in the vertical or Z direction, generally perpendicular to the front and back surfaces of the chip. Here again, only a few of the traces and vias are shown. Traces 28 and vias 30 electrically interconnect some of electronic elements 22 with one
15 another. However, the traces and vias within the chip do not provide all of the interconnections between internal elements of the chip required for the chip to function. For example, electronic element 22D must be connected to element 22C for functioning of the chip, but no internal interconnection is provided. Stated another way, chip 20 omits some or all of the internal
20 interconnections which would normally be provided in a chip of comparable design incorporating the same electrical elements. At least some of the electrical elements 22 are connected to contacts 26 on the front surface of the chip by some of the vias and traces within the chip. The assembly further includes a second semiconductor chip 32 which includes electronic
25 elements 34, vias 36, traces 38 and terminals 40 similar to the corresponding elements of first chip 20. Chip 32 has a front surface 31 and a rear surface 33. One or more auxiliary electrical components such as capacitor 42 are also provided. Capacitor 42 has terminals 44 electrically connected to its opposing plates (not shown). Other discrete components

such as resistors, inductors and active components may be provided in the same manner.

A dielectric element 50 having a top surface 52 and a bottom surface 54 is juxtaposed with chips 20 and 32 and with auxiliary element 42 so that the dielectric element overlies the front surfaces 23 and 31 of the chips. The dielectric element is also juxtaposed with the contact-bearing surface of auxiliary electrical element 42. Dielectric element 50 has numerous traces 56 and 58 extending in horizontal directions generally parallel to the top and bottom surfaces 52 and 54. The dielectric element further includes substantially continuous electrically conductive potential reference plane elements 60. Only a few traces 56 and 58 disposed in two layers are depicted in Fig. 1 and only one potential plane element 60 is shown in Fig. 1. In practice, however, the traces may be disposed in numerous layers and numerous potential plane elements may be provided. The traces and potential plane elements desirably are disposed in an alternating arrangement, so that each layer of traces lies adjacent to a potential plane element. A layer of the dielectric material of element 50 is disposed between each trace and the neighboring potential plane element 60. Further, although the traces are shown extending within the interior of dielectric element 50, some or all of the traces may be disposed on the top or bottom surfaces 52 and 54 of the dielectric element. The design of the dielectric element, including the traces 56 and 58 and potential reference planes, may be selected so that each trace, together with the neighboring potential reference plane and the intervening dielectric, define a transmission line having controlled characteristic impedance and relatively low DC resistivity. The same design rules and considerations commonly employed in design of transmission lines on circuit panels, such as thin-film multilayer interconnect circuits and circuit boards, intended to connect numerous chips or discrete elements with one another, may be employed in design of the transmission lines in dielectric element 50. Examples of the design rules and configurations used for this purpose are set forth in the

treatise, Multichip Module Technologies and Alternatives - The

Basics, Doane and Franzon, eds., 1993, pp. 259-276 and 525-567, the disclosures of which are hereby incorporated by reference herein.

Dielectric element 50 desirably is formed from a dielectric material having relatively low dielectric constant, desirably below about 4, such as polymeric material. A particularly preferred dielectric material is polyimide which has a dielectric constant of about 3.5, and which also has good dimensional stability. The traces desirably are formed from highly conductive materials such as metals having resistivity less than about 2.5 micro-ohm-cm. Gold, silver and, copper are preferred; copper and copper-based alloys are most preferred. In a multilayer traces 58 and 56 can be formed on each layer by conventional plating, etching or other patternwise forming processes. The traces typically are about 5 μm thick or more, and have widths of about 10 μm or more, most typically about 15-40 μm . Thus, traces 58 and 56 have greater cross-sectional area than the internal conductors commonly used within the chips themselves.

The coefficient of linear thermal expansion of the dielectric element 50 with the metallic traces and potential planes thereon is close to the coefficient of linear thermal expansion of the metallic materials incorporated in the traces and potential planes. Stated another way, the coefficient of thermal expansion of the dielectric element is controlled principally by the thermal expansion properties of the metallic elements. Thus, the dielectric element typically has a coefficient of thermal expansion substantially greater than the coefficient of thermal expansion of the chip. Unless otherwise specified, the term "coefficient of thermal expansion" as used herein refers to the means coefficient of linear thermal expansion (as opposed to area or volumetric expansion) unless otherwise specified. Also, unless otherwise specified the value of such coefficient is the value at about 20-30°C. Where copper is used as the metal on the dielectric element, the

dielectric element typically has a coefficient of thermal expansion greater than $10 \times 10^{-6}/^{\circ}\text{C}$, and

typically about $17 \times 10^{-6}/^{\circ}\text{C}$. By contrast, silicon chips commonly have a coefficient of thermal expansion of about $2.8 \times 10^{-6}/^{\circ}\text{C}$.

Dielectric element 50 further includes vias 62, i.e., conductors extending generally in vertical directions perpendicular to top and bottom surfaces 52 and 54. A plurality of terminals 64 are provided. These terminals are accessible at the top surface of the dielectric element so that the terminals can be connected to contact pads 76 of a substrate as further discussed below. As depicted in Fig. 1, most of the terminals 64 project outwardly from the surrounding portions of the top surface 52 of the dielectric element. However, the terminals may also be disposed in recessed portions of the top surface, such as in vias. Thus, terminal 64a is recessed relative to the surrounding portions of top surface 52, but remains exposed and accessible at the top surface through via 65.

Some or all of traces 56 and 58 are connected to terminals 26 on first chip 20 by flexible leads 66. Thus, the traces are connected to the electronic elements 22 of chip 20. At least some of the traces are connected to two or more electronic elements arranged to interchange signals with one another. For example, trace 56A and flexible leads 66A and 66B are connected between electronic elements 22C and 22D. Thus, a path for transmission of signals from element 22C and 22D extends from element 22C through internal trace 28A of the chip via 30A of the chip and then out of the chip through lead 66B, trace 56A and trace 66A back to element 22D. In similar fashion, traces 56 and 58 form parts of many additional interconnect paths between electrical elements of chip 20. Some of the traces, such as trace 56B provide connections between the first chip 20 and the second chip 32, whereas still other traces such as trace 56C provide interconnections between electronic elements of 20 and the auxiliary electronic element 42. Vias 62 and some or all of the traces may also interconnect terminals 64 with the electronic elements of the chip and with the auxiliary circuit element or

elements 42. The traces, vias and flexible leads also interconnect some of terminals 64 with potential reference planes 60 and also connect some of the contacts on each chip to these reference planes. These connections serve as ground or power connection to the assembly.

5 The assembly further includes a layer of a compliant material 70 such as a gel, foam, or elastomer, or a thermoplastic or other adhesive having a low modulus of elasticity, disposed between the bottom face 54 of the dielectric element and the chips. The flexible leads 66 extend through compliant layer 70. The assembly may further include a cover or heat sink 72
10 which may encompass some or all of the other elements of the package. Terminals 64 serve to connect the foregoing elements of the assembly to a substrate such as a circuit board or other external device 74. Thus, each terminal 64 may be connected to a corresponding contact pad 76 on substrate 74 by a mass of solder or other conventional bonding material. Each such
15 contact pad may be connected by internal circuitry 78 of the substrate to other elements of a larger circuit.

 The physical structures of the flexible leads and compliant layer may be substantially as disclosed in the aforementioned commonly assigned patents and co-pending applications. As described in said patents and co-
20 pending applications, individual portions of the chip 20 can move relative to the dielectric element without creating large mechanical stresses in the flexible leads. Thus, during operation of the system, thermal expansion and contraction of dielectric element and chip 20 may cause parts of the chip to move relative to the dielectric element 50. Such movement can be
25 accommodated without substantial mechanical stress in the flexible leads or in the dielectric element itself.

 An assembly according to a further embodiment of the invention, depicted in Fig. 2, includes only one chip 120. The dielectric element 150 has length l and width w approximately equal to the
30 corresponding dimensions of chip 120 itself. Dielectric element 150 includes

internal potential reference planes 160 and traces 156, of which a few are indicated in Fig. 2, similar to those discussed with reference to Fig. 1. In this embodiment as well, the traces of the dielectric element are connected to contacts on the chip by flexible leads 166 so that the traces and flexible leads interconnect electrical elements of the chip to one another for transmission of signals therebetween. The flexible leads also connect the terminals 164 on the top surface of the dielectric element with the chip 120. The structure of Fig. 2 provides a single unit or "tile" having all of the advantages achieved by interconnecting elements of the chip to one another through the traces of the dielectric element.

Particularly preferred methods of making assemblies with large numbers of flexible leads interconnecting contacts on a chip and conductors on a dielectric element are disclosed in the aforementioned U.S. Patent 5,518,964 and WO 96/02068. Briefly, in preferred methods according to these patents and applications, each flexible lead has a first or terminal end permanently attached to the dielectric element and a second or tip end releasably attached to the dielectric element. The dielectric element is juxtaposed with the chip and the tip ends of the leads are bonded to the contacts on the chip, whereupon the chip and dielectric element are moved away from one another to release the tip end of each lead from the dielectric element and deform the leads in a controlled manner to a vertically-extensive configuration. The compliant layer may be formed by injecting a flowable material between the chip and the dielectric layer and then curing the flowable material to form the compliant layer. In a variant of this process, the leads are initially provided on the surface of the chip and bonded to contacts on the dielectric elements. These processes may be performed while the chip is present as part of a wafer. The wafer-level process can be used, for example, to make single chip tiles as depicted in Fig. 2. The flexible leads may be configured as flexible loops attached at

one point of the loop to the chip contact and attached at another point of the loop to the conductive feature of

the dielectric element to provide a low-inductance connection between the chip contacts and the conductive traces and vias of the dielectric element. As taught in International Publication No. WO 97/11588 published 27 March 1997, the disclosure of which is hereby incorporated by reference herein, each
5 flexible lead may include both a principal conductor and a reference conductor, and a dielectric material intervening between the principal conductor and the reference conductor, so that the lead itself provides a controlled-impedance transmission line. The principal conductor of each such lead may be electrically continuous with one of the traces 56 or 58, whereas
10 the reference conductor of each such lead may be continuous with one of the potential plane elements 60.

The particular arrangement of interconnections between the various elements depends upon the circuit design of the particular chip or chips. However, the electrical elements of each chip which are interconnected
15 with one another through the traces 56 or 58 of the dielectric element desirably include clock-timed elements arranged to send and receive signals to one another as digital signals through the traces of the interconnect element in synchronism with a common clock such as the internal clock of the chip itself. Thus, typical digital electronic chips operate cyclically. An electronic
20 element must react to the signal which it received during the previous clock cycle and send a signal to an associated element so that the receiving element obtains the new signal in usable form before the end of the clock cycle. Thus, the required cycle time for any pair of elements includes the internal operation time of the element which sends the signal, plus the transmission time
25 required for the signal to reach a stable value at the receiving element after the sending element operates. The time for each cycle of the clock cannot be less than the longest required cycle time for any pair of elements controlled by the clock.

As described in the aforementioned Doane and Franzon treatise,
30 the signal transmission time or $t_{\text{interconnect}}$ includes both signal propagation time

and settling time. Signal propagation time or t_{prop} is the time required for the voltage at the receiving end of the transmission line to rise for the first time after the voltage at the sending end of the transmission line rises. Settling time or t_{settle} is a measure of the time required for voltage oscillations due to reflections and noise in the transmission line to dissipate. The electrical characteristics achievable in the controlled impedance paths provided by the traces of the dielectric elements can provide equal or, preferably, shorter interconnect times than those which are achievable in purely internal circuitry within the chip itself. Typically, the dielectric material of the dielectric element 50 has a lower dielectric constant than the dielectric material of the chip itself, which tends to provide a higher signal propagation speed along the paths provided by the traces than along the internal traces 28 of the chip itself. The traces on the dielectric element may have width and thickness optimized to provide short interconnect times. Thus, the dimensions of the internal traces of the chip are constrained both by the limited space available within the chip itself and by the limitations of chip-fabrication processes. Typically, these internal traces within the chip are on the order of one micron or less in width and thickness. The internal traces thus have a high resistance, which tends to lengthen the settling time. Moreover, the space within the chip is occupied by the electronic elements themselves, so that the internal traces often must take tortuous paths which increases the physical length of each trace and thereby increases the propagation time. By contrast, the dielectric element can provide traces of substantially greater width and thickness than the internal traces within the chip, and which therefore have lower resistance. Also, the traces on the dielectric element can follow routings which are close to optimum. Moreover, typical internal traces are formed from highly resistive metals such as aluminum, which further aggravates the problem of high resistance, whereas the traces on the dielectric element are conveniently formed from metals of lower resistivity such as copper or gold. Additionally,

almost any number of layers of traces can be provided on the dielectric element.

In many cases it is impossible to provide controlled characteristic impedance along the length of an internal trace within the chip.

5 Thus, in many cases the internal conductors 28 within the chip have marked variations in characteristic impedance along their length. This leads to signal reflections along the leads and increased settling time. The traces 56 and 58 of the dielectric element, in conjunction with the potential reference elements 60 and the dielectric intervening between each trace and the neighboring

10 potential reference elements provide controlled, desirably constant characteristic impedance along the length of each trace. This minimizes signal reflections along the length of the trace and greatly reduces the settling time associated with the interconnection.

Thus, where some or all of the interconnections between

15 electronic elements of the chip are made through the traces of the dielectric element, the clock speed of the chip may be increased above the clock speed which would be possible using only interconnections within the chip itself. It is not necessary to make all of the interconnections between elements of the chip through the traces on the dielectric element in order to achieve such an

20 increase. Typically, in a given chip design, a few interconnections pose the most critical problem. Interconnections between widely separated elements of the chip or interconnection which require difficult, tortuous routings between chip elements may have longer interconnect times than other interconnections within the same chip. Because the clock speed of the entire chip is limited by

25 the longest interconnect time, rerouting of these few critical interconnections through the traces of the dielectric element can allow operation at a higher clock speed. These advantages are particular important where the chips operate at relatively high clock speeds as, for example, at clock frequencies above about 100 MHz, more preferably above about 200 MHz and most

30 preferably above about 300 MHz or more. In particular, certain chips are

arranged to operate at clock speed of 500 MHz and, in some cases, above 800 MHz, with some of the most advanced chips having clock speeds above 1GHz. The advantages of the present invention are more pronounced at such high clock speeds.

5 As illustrated in Fig. 3, traces within a dielectric element may be provided as pairs of traces such as traces 258a and 258b extending parallel to and adjacent one another. Traces 258a and 258b may overlie a common potential reference plane 260. Paired traces 258a and 258b are connected to a electronic elements 222a and 222b so that both traces of the pair interconnect
10 the same electronic elements. The paired traces 258a and 258b provide a multiconductor transmission line. The transmission line has a first end 261 and a second end 263 disposed at spaced apart locations on the dielectric element. At each end, the conductive features or traces 258a and 258b constituting the transmission line are connected to an electronic element 222
15 of the chip through a set of deformable conductive elements or flexible leads extending between the traces and a set of closely spaced contacts on the chip. Thus, traces 258a and 258b are connected at end 261 through a pair of flexible leads 262a and 262b to a pair of adjacent contacts 266a and 266b on the front surface of the chip. Contact 266a and 266b in turn are connected to
20 electronic element 222a. Similarly, at end 263 the traces are connected to contacts 267 through a further pair of flexible leads 265. Contacts 267 in turn are connected to internal electronic element 222b of the chip. The term "adjacent-connected end" as used in this disclosure refers to an end of a transmission line at which a plurality of conductive features incorporated in
25 the transmission line are connected to a plurality of adjacent contacts on the chip. Preferably, the chip contacts of each such adjacent-connected end are within about 1000mm center-to-center.

 The electronic elements connected to the ends of the transmission line or paired traces are adapted to transmit signals between them
30 through the paired traces. Thus, element 222a may be arranged to send

signals to element 222b by applying a positive-going voltage on trace 258a and a negative-going voltage on trace 258b or vice versa. Alternatively, trace 258a may serve as a local ground whereas trace 258b may serve as the signal carrying trace. The receiving element 222b may be arranged to detect as the
5 signal the difference between the voltages on traces 258a and 258b. This arrangement provides substantial reduction in electromagnetic noise and crosstalk from adjacent signal paths.

The structure depicted in Fig. 4 includes a transmission line 200 incorporating three parallel conductors 202a, 202b and 202c extending on a
10 dielectric sheet 204. These particular conductors do not extend in proximity to any ground or other constant potential plane. At the end of the transmission line shown in Fig. 4, conductors 202a, 202b and 202c are connected to a set of three adjacent contacts 206a, 206b, 206c on the chip surface by a set of three independent flexible metallic leads 208a, 208b, 208c.
15 The compliant layer 210, which closely surrounds leads 208 is partially removed in Fig. 4 for clarity of illustration. The center trace or conductive element 202b is connected through terminal 206b to a signal terminal 206b of an internal electronic element 212 within the chip, so that the center trace serves as the signal conductor, whereas the side traces 202a and 202c act as
20 return paths. Thus, traces 202a is connected through lead 208a and terminal 206a to a local ground connection of electronic element 212 of the chip. The opposite external trace 202c is connected through a lead 208c and terminal 206c to a power or system supply voltage connection of the same electronic element 212. A similar connection (not shown) is provided at the other end of
25 transmission line 200. A transmission line incorporating three adjacent conductors, one connected to a signal and the others connected to power and ground respectively is commonly referred to as a "tri-lead" transmission line. A tri-lead transmission line provides current return paths for signals of either
30 polarity. For a signal of one polarity (rising voltage on the signal trace) the return current will flow along one of the outside traces, whereas for the

opposite polarity signal (falling voltage on the signal trace) the return current will flow along the other exterior trace. The conductors of transmission line 200 typically are arranged to provide a characteristic impedance along the transmission line of about 20 -160 Ohms , as for example, from about 20- to
5 about 100 Ohms. The conductors constituting the traces typically have a width W of about $25\mu\text{m}$ - $50\mu\text{m}$, whereas the spaces between the conductors typically have a width S of about $25\mu\text{m}$ - $75\mu\text{m}$ and more typically about $50\mu\text{m}$ - $75\mu\text{m}$. Here again, the traces when formed from copper, typically are more than about 5 microns thick.

10 The leads connecting the various traces 202 to the contacts at the end of the trace shown in Fig. 4 extend substantially parallel to one another. That is, each lead 208 extends downwardly from the dielectric film to the chip surface in the vertical or Z direction and curves in the horizontal or X and Y directions. The leads have a nested configuration, so that the convex
15 side of each curving lead faces toward the concave side of the neighboring lead. The distance between the leads remains substantially constant over the entire lengths of the leads. Thus, the leads constitute an extension of the transmission line, without an abrupt change in characteristic impedance at the juncture between the leads and the traces. As mentioned above, the compliant
20 material 210 closely surrounds the leads. To further minimize changes in characteristic impedance at the juncture of the leads and traces, the dielectric constant of the compliant material may be selected to match that of the flexible dielectric layer 204.

The layout of the conductors constituting transmission line 200
25 adjacent to one another minimizes the area encompassed by a loop including the signal conductor and any single return path, *i.e.*, the loop including center conductor 202b and exterior conductor 202a, or the loop including center conductor 202b and exterior conductor 202c. This in turn minimizes the effect of electromagnetic interference on the signals sent through the

transmission line. The effect of a changing magnetic field is directly related to the integral of the change in field over the area encompassed by the loop. The same layout also minimizes electromagnetic radiation from the transmission line. The flexible leads or deformable conductive elements 208
5 which connect the transmission line to the contacts on the chip form part of the loop. The use of physically parallel leads extending to closely spaced contacts on the chip further minimizes the area encompassed by each signal loop. The dual-conductor transmission line discussed above with reference to Fig. 3 provides similar effects. The leads associated with the dual-conductor
10 line can be configured in an arrangement similar to that shown in Fig. 4.

As shown in Fig. 5, a first multiconductor transmission line 240 includes a trace 242 extending on one side of a dielectric layer 244 and an electrically conductive potential plane element 246 on the opposite side of the dielectric layer, the trace and potential plane element cooperatively defining a
15 multiconductor transmission line in the form of a stripline. The two conductive elements of this transmission line (the potential plane element and the trace) are connected by leads 249 at an end 248 of the transmission line to an electronic device 250 within the chip. The conductive elements of the transmission line are similarly connected to a further electronic element (not
20 shown) of the chip at the other end of the transmission line. One or more additional transmission lines also incorporate the same conductive potential plane 246. Thus, conductor 252 and potential plane 246 cooperatively define a further transmission line 254, which is connected between an separate electronic element 256 of the chip at the end visible in Fig. 5 and another
25 element (not shown) at the other end of line 254.

A further transmission line 270 is formed by a pair of traces 272 and 274 extending on opposite sides of a dielectric layer 276 (Figs. 6 and 7). The conductive elements or traces 272 and 274 included in the transmission line are connected by a single plural-conductor lead 275. The lead includes a
30 dielectric strip 277, which may be formed integrally with dielectric layer 276,

a first conductor 278 continuous with trace 272 and a second conductor 279 continuous with trace 274. In effect, the multiconductor lead is configured as an extension of the dielectric element, projecting from the main body of the dielectric element. The multiconductor lead is flexible so that the distal or tip end of the lead remote from the main body, is movable independently of the remainder of the dielectric element. At the distal end of the lead, the conductors of the multiconductor lead are attached to contacts 280 and 282, thereby connecting the conductive elements of the transmission line to an electronic element 284 of the chip. The bonds between the lead conductors and the contacts may be made by techniques such as thermal activation of a bonding material such as a solder, diffusion bonding alloy, eutectic bonding alloy or other fusible composition. The bond also can be made by techniques such as compression, thermocompression, sonic, thermosonic or ultrasonic bonding. Where the bonding technique requires access to the top surfaces of both conductors for direct engagement of a bonding tool with the conductor surface, a hole 288 may extend through the upper conductor 279 and dielectric strip 276 at or near the distal end of the lead, so that a bonding tool can be inserted in the hole to engage the upper surface of lower conductor 278.

A similar connection can be provided at the opposite end (not shown) of the transmission line. The dimensions of the multiconductor lead may be selected to provide characteristic impedance identical or nearly identical to the characteristic impedance of the transmission line itself. Moreover, the conductors of the multiconductor lead are closely juxtaposed with one another, thereby minimizing the area within the signal loop. A multiconductor lead may include more than two conductors. For example, a multiconductor lead for use with a tri-lead transmission line may include three conductors. Also, the conductors of a multiconductor lead may extend alongside one another rather than on top of one another.

The transmission line 290 of Fig. 8 includes a conductor 292 and potential plane 291 defining a stripline as discussed above in connection

with Fig. 5, the conductive elements of the stripline being connected to a first electronic element 293 of the chip through a multiconductor lead as discussed above with reference to Figs. 6 and 7. Element 293 is arranged to send signals along the first transmission line or stripline 290. Transmission
5 line 290 branches to form two further transmission lines 294 and 295. As further discussed below, the branching transmission lines have dimensions selected to provide an aggregate characteristic impedance in both branches equal to the characteristic impedance the main line 290. Line 294 extends to another element within the chip, whereas the signal conductor 296 of line
10 295 extends to a terminal 297 accessible at the top surface of the dielectric element (the surface facing away from the chip) so that terminal 297 is available for connection to an external signal path in the same manner as the terminals 64 discussed above with reference to Fig. 1. A further terminal 298 connected to potential plane 291 may be provided for connecting the
15 potential plane so that the multiconductor signal path may continue in the external substrate to which the assembly is mounted.

The structures discussed above may include interconnections between essentially any electronic elements of the chip, as well as connections to external devices. However, it is particularly advantageous to
20 use the conductive elements on the dielectric element to connect the internal data cache or "cache memory" of a microprocessor chip, or the data-receiving or data-sending interface of the cache memory, with the actual data processing units of the chip, such as the logic unit or an interface associated therewith. Such interconnection requires numerous parallel signal
25 paths all capable of operating at the clock-speed of the chip to provide parallel transfer of, *e.g.*, 16, 32, 64, 128 or 256 bits of data in each clock cycle. Moreover, the data cache and the logic unit may be separated from one another by a substantial distance on the chip and other components may be disposed between them.

A further particularly preferred embodiment of the present invention utilizes transmission lines on the dielectric element to distribute the

timing signals from the internal clock of the chip to the clock-timed elements of the chip. Thus, as depicted in Fig. 9, the electronic elements of the chip may include an internal clock 302 connected to a contact 304 and adapted to send clock signals through that contact. Contact 304 in turn is connected to a primary or central conductive transmission line defined by trace 306 on the dielectric element 308 and a potential reference plane (not shown). The signal path defined by the central trace has a first characteristic impedance or Z_0 . Each end of the central trace is connected to n_2 secondary traces 310. In the embodiment illustrated, n_2 is two at both ends of primary trace 306, and hence two secondary traces connect to each end of the primary trace. The characteristic impedance of each secondary trace is equal to n_2 times the characteristic impedance of the primary trace. Stated another way, the aggregate characteristic impedance of the secondary transmission lines connected at each end of the primary transmission line is equal to the characteristic impedance of the primary transmission line itself. This arrangement minimizes signal reflections at the end of the primary trace. Similarly, n_3 tertiary transmission lines 312 are connected at each end of each secondary transmission line. The characteristic impedance of each tertiary line is n_3 times the characteristic impedance of each secondary line 310. Similarly, n_4 quaternary lines 314 are connected at each end of each tertiary trace and the characteristic impedance of each quaternary line is n_4 times the characteristic impedance of the connected tertiary line. The traces included in Quaternary lines 314 are connected typically through flexible leads and/or vias to contacts 316 of the chip. These contacts are connected to internal clock conductors or "clock drops" of the chip. Internal conductors may connect each contact 316 directly to a clock-timed element 318 or, alternatively, the internal conductors of the chip may further branch and may connect contact 316 to several clock-timed internal elements 318.

Thus, the transmission lines of the dielectric element form a branching structure such that at each end of a high-level line, the next lower-

level lines provide an aggregate impedance equal to the impedance of the high level line. This arrangement substantially suppresses reflections at the ends of the lines and thus substantially suppresses signal reflections in the traces used to carry the clock signals. The ability to provide controlled impedances in the

5 transmission lines allows construction of such a substantially reflection-free signal path. A similar arrangement can be used for distribution of other signals from a single source or transmitter to numerous receivers. In examples of an arrangement where n_2 , n_3 , n_4 are each two, the characteristic impedances of the primary, secondary, tertiary and quaternary traces can be either 20, 40,

10 80 and 160 ohms, respectively, or 10, 20, 40 and 80 ohms, respectively. The arrangement can be varied so as to use fewer levels of transmission lines as, for example, to connect the tertiary lines directly to the clock drop or to use more levels of traces. Also, n_2 , n_3 and n_4 can have integer values other than 2. Also, the values of n_2 , n_3 and n_4 need not be uniform throughout the branching

15 structure; the number of lower-level lines connected at one end of a higher-level line may differ from the number of lower-level lines connected at the other end, but at each end the aggregate characteristic impedance of the lower-level lines (considered as parallel to one another) should be equal to the characteristic impedance of the higher-level line. Within a given layer, the

20 characteristic impedances of transmission lines formed by traces overlying potential planes are approximately inversely proportional to the width of the trace. Thus, as depicted in Fig. 9, the primary trace is very wide, the secondary traces are narrower and so on. Further, it is possible and in some cases preferable to have multiple clock branching structure layers within the

25 dielectric substrate. Individual clock branching structure layers can carry the same clock signals or different clock signals, with respect to the other clock branching structure layers, to respective electronic elements within the chip.

An assembly according to a further embodiment of the invention (Fig. 10) includes masses of a fusible, electrically conductive material 466

30 connected between the terminals 440 of chips 420 and 432 and the conductive

contacts 443 on the bottom surface 454 of dielectric element 450. Additional masses 440 of fusible conductive material extend between terminals 444 of an additional electrical element such as a capacitor and further contacts 443 on the dielectric element. A layer of a compliant dielectric material 470 such as a gel, elastomer or foam extends between the dielectric element 450 and the chips and additional electrical element. The compliant dielectric material intimately surrounds each mass of fusible conductive material such as a relatively low-melting metal or metal alloy. The fusible conductive material has a melting temperature which preferably is within or below the range of operating temperatures of chips 420 and 432. Desirably, the melting temperature is less than about 150°C, preferably less than about 125°C and more preferably less than about 100°C. Melting temperatures below about 85°C are more preferred, and melting temperatures below about 65°C are even more preferred. The range of melting temperatures between about 25°C and 65°C is particularly preferred, and melting temperatures between about 35°C and about 55°C are especially preferred.

During operation of the assembly, the fusible masses reach melting temperature and become wholly or partially liquid. The molten fusible material in each mass is confined by the surrounding compliant dielectric material 470. In this condition, the molten fusible material continues to maintain electrical conduction between the terminals of the chips and the conductive contacts of the dielectric element. However, the molten fusible material offers essentially no resistance to deformation. The fusible material thus serves as deformable electrically conductive element, in place of the flexible leads discussed above. Moreover, the fusible material masses provide contacts which have low resistance and which also have low self-inductance, and therefore have low impedance even at high frequencies. To minimize the inductance of the masses, they are preferably formed as solid, generally spherical or cylindrical bodies.

Microelectronic assemblies and devices utilizing fusible conductive materials, as well as methods of making such assemblies, are described in greater detail in International Patent Publication WO 97/40958 the disclosure of which is incorporated by reference herein. As further set forth in the '958 Publication, the contacts of the chip and dielectric element may be provided with barrier layers which are resistant to alloying with the molten fusible material. The masses of fusible material may be applied to one of the elements to be interconnected, such as to the chip or to the dielectric element, using techniques similar to those used to apply conventional solder masses. The elements may then be juxtaposed with one another and heated to reflow the fusible material onto the contacts. A curable liquid material may then be introduced around the fusible material and cured to form the compliant material.

As also set forth in the '958 Publication, the fusible material may be adapted to melt during processing steps. For example, where the contacts 464 of dielectric element 450 are connected to pads 476 on a substrate, fusible masses 466 may be arranged to melt during the bonding process. This allows movement of the dielectric element 450 during bonding, so as to compensate for any deviation of contacts 464 or pads 476 from planarity. This capability is particularly useful where dielectric element 450 is a flexible, sheetlike element such as a flexible polyimide structure.

As discussed above with reference to terminals 64 (Fig. 1) ; 297 and 298 (fig. 8) and 464 (Fig. 10) terminals may be provided to connect the assembly to external circuitry. The aforementioned Patents, PCT publications and patent applications disclose numerous arrangements and patterns of leads and traces which connect contacts on the chip to terminals on a dielectric element. Any of these patterns can be incorporated in an assembly according to the teachings of the present invention. For example the leads and traces associated with the terminals can "fan-in" or extend inwardly from contacts at the periphery of the chip to terminals overlying the central

region of the chip. Also, the traces associated with terminals can "fan-out" or extend outwardly beyond the periphery of the chip. A "fan-in - fan-out" structure which has some leads and traces extending inwardly to terminals on a central region of the structure and also has other leads and traces extending
5 outwardly to terminals on a peripheral region of the structure. Any of these structures can be made in accordance with the present invention.

A component in accordance with a further embodiment of the invention (Fig. 11) includes a multilayer dielectric support structure. The support structure includes potential plane elements 920 and 921 adjacent the
10 top and bottom of the structure, and further includes internal traces 934 and 935 disposed at various layers within the substrate. Although only two potential plane elements and two layers of traces are illustrated in Fig. 11, it should be appreciated that, in practice, the structure may include numerous layers of traces and more or fewer potential plane elements. Typically, the
15 traces within each layer extend generally parallel to one another. Pairs or triplets of traces in a single layer may define dual-lead or tri-lead transmission lines as discussed above with reference to Figs. 3 and 4, whereas traces in superposed layers may define transmission lines as shown in Figs 6 and 7, and a trace and a potential plane may define stripline transmission lines as shown
20 in Fig. 4. A transmission line may also include plural traces and one or more potential planes. In the structure of Fig. 11, the two layers of traces 934 and 935 depicted in the drawing have traces extending in the same direction. Other layers (not shown) have traces extending in perpendicular directions, into and out of the plane of the drawing as seen in Fig. 11. The connection
25 component has numerous plural conductor leads 936 distributed in an "area array" pattern on the bottom surface of the support structure so that the pattern of leads covers a substantial area on the bottom of the structure. Each plural conductor lead includes a flexible dielectric, preferably polymeric dielectric strip 941, a first conductor 950 overlying the top surface of the polymeric

strip and a second conductor 948 overlying the opposite, bottom surface of the strip, *i.e.*, the surface of the strip facing away from support structure 912.

A first or fixed end 938 of each lead 936 is permanently attached to the support structure 912. A first metallic vertical conductor or via 939 connects the first conductor 950 of lead 936a to a trace 935 in one layer, whereas a second vertical conductor 943 at the first end 938 of the lead connects the conductor 948 with a further trace 934 within the support structure. The vertical conductors are electrically isolated from one another and from other conductive structures on the support structure as, for example, from the potential plane element 921 on the bottom surface. Also, the second via 943 extends through the polymeric strip 941 of the lead. Again, the particular set of traces depicted in Fig. 11 is merely representative of the numerous traces included in a multilayer structure. Thus, the vias at the fixed ends of the leads 936 may be connected to traces in different layers; to different traces in the same layer or to traces and potential planes. Preferably, however, the two vias associated with each lead are connected to conductive features, such as traces 934 and 935, which cooperatively define a transmission line with a controlled, characteristic impedance along its length. Some leads may have one or both of the vias associated with the lead connected to other conductive elements on the support structure as, for example, to terminals on the top surface of the support structure. Also, the vias 939 and 943 associated with each plural-conductor lead need not be side-by-side as illustrated. For example, the vias associated with each double connection lead may include a hollow via, and a further via inside the hollow via.

The second or tip end 940 of each double connection lead 936 is releasably connected to the bottom surface of the support structure. The releasable connection is arranged so that it is strong enough to hold the tip end of the lead in place from the time the component is manufactured until the component is used, but is weak enough that the connection can be readily

broken by pulling the lead away from the bottom surface of the support structure. In the particular arrangement shown in Fig. 11, the first trace 950 is provided with a small metallic "button" 945 adjacent its tip end. This button weakly adheres to a dielectric layer 947 on the bottom surface of the support structure. As described in greater detail in the aforementioned '964 patent, metallic "buttons" of this nature can be formed by an etching process in which a relatively readily etchable metal such as copper is attached by an etchant which does not substantially attack the metal of the lead. Other structures which releasably secure the tip ends of the leads to the support structure may be employed. For example, metallic button 945 may be replaced by a polymeric connector of small cross-sectional area, such as a polymeric connector having widthwise dimensions smaller than the width of the lead. Such a polymeric connector may be readily broken by pulling the lead tip end away from the bottom surface of the support structure. Polymeric connecting elements of this nature can be formed by etching a polymer layer beneath the leads using the leads as etch stops so as to leave a small connecting element. This process can be performed, for example, by plasma etching in an oxygen-containing plasma.

At the tip end of each plural conductor lead, an electrically conductive, preferably metallic via liner 953 projects downwardly from the first conductor 950 through the polymeric dielectric strip 941. A mass 969 of an electrically conductive bonding material, which preferably is a heated-activatable bonding material as discussed above is provided on the bottom end of via 953. A mass 971 of a similar bonding material is provided at the distal end of the second conductor 948. The distal end of the second conductor terminates proximally of via 953 and mass 969, so that the tip end of the second conductor 948 remains electrically insulated from the first conductor 950 and via 953.

The component also has terminals 924 and 925 on the top surface of support structure 912. These terminals may be connected to some

of the internal traces 934 and 935, as by vertical conductors or vias 926 and 927, respectively. The terminals preferably are provided in sets such as pairs or triplets, with the terminals of each set being connected to a set of electrically conductive features such as co-directionally extending traces, or a trace and potential plane, which cooperatively define a transmission line.
5 Other terminals 924 and 925 may be connected to other electrically conductive features such as directly to the vias 943 and 939 associated with the leads, or to isolated potential plane elements or isolated traces.

The component of Fig. 11 may be connected to a
10 microelectronic element such as a semiconductor chip 962, as depicted in Fig. 12. In the connection process, the bottom surface of the connection component, with leads 936 thereon is juxtaposed with the top surface of the chip so that bonding material masses 969 and 971 on the tip ends of each lead are aligned with contacts 966 and 967 on the microelectronic element. The
15 support structure and microelectronic element are engaged with one another under heat and pressure so that the bonding material masses 969 and 971 at the tip ends of the lead are activated to bond the via 953 (Fig. 11) associated with the first conductor 950 of each lead to a terminal 966 on the microelectronic element and to bond the second conductor 948 to another
20 contact 967 of the same contact pair on the microelectronic element. The support structure and microelectronic element are moved away from another to deform the leads through a preselected displacement and to detach the tip end of each lead from the support structure and to deform the leads into the vertically extensive configuration depicted in Fig. 12. A compliant, dielectric
25 encapsulant 960 is injected and cured between the support structure and the microelectronic element.

The resulting structure incorporates leads and traces in support structure 912 which interconnect two or more electronic devices 971 within the same microelectronic element or chip. The individual devices connected
30 to one another by the interconnected traces and leads may be connected in a

differential signal or tri-lead arrangement of the types described above. Here again, sets of closely spaced contacts may be associated with each device, and these pairs may be interconnected to one another by parallel conductive paths. For example, devices 971a and 971b are connected to one another by a
5 multiconductor-transmission line constituted by the conductors of leads 936a and 936b and by traces 934a and 935a within the support structure. The transmission line extending between the devices has well controlled impedance over substantially all of its length and provides rapid, predictable signal transmission. The connected devices may also be connected to the
10 terminals 924 and 925 on the top surface of the dielectric support structure as schematically depicted in Fig. 12.

The process of applying the dielectric layer and deformable conductive elements can be conducted using an individual chip, or else can be conducted while the semiconductor chip is part of a unitary semiconductor
15 structure such as a wafer. For example, a unitary wafer 980 (Fig. 13) includes a plurality of individual semiconductor chips 982. A set of individual dielectric elements 984 with conductive features thereon can be connected to the various chips in the manner described above and connected to the chips. After such connection, and preferably after introduction of a compliant
20 material between the chips and dielectric elements, the wafer is severed so as to provide individual units as depicted in Fig. 2. Alternatively, the dielectric elements 990 may be provided as parts of a unitary dielectric structure 986 (Fig. 14). This unitary structure is assembled to the wafer and the contacts on the chips in the wafer are connected to the conductive features of the unitary
25 structure through the deformable conductive elements. Preferably, a compliant layer is introduced between the unitary structure and the wafer. The assembly is then severed so as to sever both the unitary structure and the wafer and provide individual units each including a chip and an dielectric element.

Deformable conductive elements other than the specific types mentioned above can also be employed. For example, flexible electrically conductive polymers or polymer compositions may be utilized. As used in this disclosure, the term "deformable conductive element" should be understood as referring to a conductive element which is either fluid or else substantially more flexible than the parts to which it is connected, so that the conductive element tends to deform to a greater degree than the parts of the structure physically connected to the conductive element when the structure is deformed. Also, a deformable conductive element which is flexible should be considerably more flexible than a typical solder ball. The preferred flexible conductive elements are elongated leads, having a long dimension several times that of their shortest dimension, so that the elongated leads can deform in bending with bending strain distributed over a substantial portion of the length of the lead. Moreover, a deformable conductive element as referred to herein should not undergo plastic deformation or stressed beyond its fatigue limit stress when subjected to thermal cycling of the assembly over typical operating and storage temperatures as, for example, -40°C to 85°C. The term "fatigue limit stress" as referred to herein means the stress which the material will fail in fatigue at an 10,000 cycles. Where elements vary substantially in physical properties with temperature (such as certain fusible conductive elements discussed above), the determination of whether a conductive element is or is not deformable should be made on the basis of its properties at the maximum normal operating temperature of the chip. Typical silicon-based semiconductor elements are designed to operate at about 40°C to about 85°C.

As these and other variations and combinations of the features discussed above can be utilized without departing from the present invention, the foregoing description of the preferred embodiments should be taken by way of illustration rather than by way of limitation of the invention as defined by the claims.

INDUSTRIAL APPLICABILITY

The present invention can be applied in manufacture of electronic devices.

CLAIMS:

1. A microelectronic assembly including:
 - (a) a first semiconductor chip including a plurality of electronic
5 elements adapted to receive and send signals and a front surface having
contacts thereon, at least some of said electronic elements being connected to
said contacts;
 - (b) a dielectric element separate from said chip and movable with
respect to said chip, said dielectric element having a plurality of conductive
10 interconnect traces thereon; and
 - (c) deformable conductive elements interconnecting said at least some
of said contacts with said interconnect traces so that at least some of said
electronic elements are connected to one another for transmission of signals
therebetween through said traces..
- 15 2. An assembly as claimed in claim 1 wherein said dielectric element and
said first semiconductor chip have different coefficients of thermal expansion.
3. An assembly as claimed in claim 2 wherein said chip is formed
20 predominantly from silicon and said dielectric element has a coefficient of
thermal expansion greater than 10×10^6 cm/cm/°C.
4. An assembly as claimed in claim 2 wherein said dielectric element
includes a polymeric body having said traces thereon and wherein said traces
25 are metallic.
5. An assembly as claimed in claim 1 wherein said deformable conductive
elements include flexible leads.

6. An assembly as claimed in claim 1 wherein said deformable conductive elements include masses of a fusible electrically conductive material having a melting temperature below about 150°C.
- 5 7. An assembly as claimed in claim 6 wherein said chip is adapted to operate in a range of operating temperatures up to a maximum operating temperature and said melting temperature is at or below said maximum operating temperature.
- 10 8. An assembly as claimed in claim 6 further comprising a compliant dielectric material surrounding said masses and confining said fusible material when said fusible material is in a molten state.
- 15 9. An assembly as claimed in claim 1 further comprising a compliant dielectric layer disposed between said dielectric element and said chip.
10. An assembly as claimed in claim 9, wherein said dielectric element overlies said front surface of said first semiconductor chip, said compliant layer being disposed between said front surface of said chip and said
20 dielectric element.
11. An assembly as claimed in claim 1 or claim 10 wherein said dielectric element has a bottom surface facing toward said first chip, a top surface facing away from said first chip, and a plurality of terminals accessible at said
25 top surface, said terminals being connected to said chip by said deformable conductive elements.
12. An assembly as claimed in claim 11 further comprising a substrate having electrically conductive elements therein, said terminals on said

dielectric element being electrically connected to the conductive elements of said substrate.

13. An assembly as claimed claim 1 further comprising a second
5 semiconductor chip having electronic elements therein juxtaposed with said dielectric element, the electronic elements of said second chip being connected to at least some of said traces.

14. An assembly as claimed in claim 13 wherein some of said traces and
10 said interconnect electronic elements of said first and second chips with one another.

15. An assembly as claimed in claim 1 or claim 10 further comprising an auxiliary circuit element juxtaposed with said dielectric element and
15 connected to at least some of said traces, at least some of said traces connecting electronic elements of said first chip to said auxiliary circuit element.

16. An assembly as claimed in or claim 1 or claim 10 wherein said traces
20 have resistivity less than 2.5 microohms -cm.

17. An assembly as claimed in claim 16 wherein said traces include one or more metals selected from the group consisting of gold, silver, copper and alloys thereof.

25

18. An assembly as claimed in claim 17 wherein said traces include copper.

19. An assembly as claimed in claim 16 wherein said traces are at least
30 about 10 μ m wide and at least about 5 μ m thick.

20. An assembly as claimed in claim 16 wherein said dielectric element includes a dielectric material having dielectric constant of less than about 4.
- 5 21. An assembly as claimed in claim 20 wherein said dielectric material consists essentially of polyimide.
22. A microelectronic assembly including:
- 10 (a) a first semiconductor chip including a plurality of electronic elements adapted to receive and send signals and a front surface having contacts thereon, said electronic elements including an internal clock adapted to generate periodic clock signals and a plurality of clock-timed elements operable in response to said clock signals said clock being connected to at least one of said contacts, said clock-timed elements being connected to others
- 15 of said contacts;
- (b) a dielectric element separate from said chip, said dielectric element having a plurality of conductive interconnect traces thereon, at least some of said contacts being connected with at least some of said interconnect traces so that said clock is connected to said clock-timed elements one for transmission
- 20 of said clock signals through said traces from said clock to said clock-timed elements.
23. An assembly as claimed in claim 22 wherein said internal clock is operative to provide clock signals at a frequency of at least 300 MHz.
- 25 24. An assembly as claimed in claim 22 wherein said dielectric element includes transmission lines incorporating said traces, said transmission lines including include a central transmission line connected to said clock, n_2 secondary transmission lines connected to said central transmission line at an
- 30 end thereof, and n_3 tertiary transmission lines connected to at least one said

secondary transmission line at least one end thereof, each said transmission line having a characteristic impedance, the characteristic impedance of each said secondary transmission line being about n_2 times the characteristic impedance of said primary transmission line, the characteristic impedance of
5 each said tertiary transmission line being about n_3 times the characteristic impedance of each said secondary transmission line.

25. An assembly as claimed in claim 24 wherein n_2 and n_3 are each 2.
- 10 26. An assembly as claimed in claim 24 wherein n_2 secondary transmission lines are connected to said central transmission line at each end thereof and wherein n_3 tertiary transmission lines are connected to each end of each said secondary transmission line.
- 15 27. An assembly as claimed in claim 22 wherein said traces include at least one set of paired traces extending substantially parallel to one another and adjacent to one another, said electronic elements including at least one sender-receiver pair connected by both traces of one said set of paired traces.
- 20 28. An assembly as claimed in claim 22 wherein said dielectric element includes one or more conductive potential reference elements juxtaposed with said traces but separated therefrom by dielectric material of said dielectric element so that said traces and potential reference elements cooperatively define controlled impedance transmission lines.
- 25 29. An assembly as claimed in claim 28 wherein said potential reference elements include one or more conductive reference planes.

30. An assembly as claimed in claim 29 wherein said traces are arranged in a plurality of layers, said one or more reference planes extending parallel to said layers of traces.

5 31. A microelectronic assembly including:

(a) a first semiconductor chip including a plurality of electronic elements adapted to receive and send signals and a front surface having contacts thereon, at least some of said electronic elements being connected to said contacts;

10 (b) a dielectric element separate from said chip, said dielectric element having a plurality of conductive features thereon, said conductive features including at least one set of plural conductive features defining a multiconductor transmission line extending between spaced-apart locations on said dielectric element, said electronic elements of said chip including at least
15 one pair of multiply-connected elements, each said pair of multiply-connected elements being connected to one another through the plural conductive features of one said transmission line.

32. An assembly as claimed in claim 31 wherein at least one said
20 transmission line is arranged so that any two conductive features of that transmission line define a mean distance therebetween less than about 100 μm .

33. An assembly as claimed in claim 31 wherein said conductive features
25 of at least one said transmission line include two or more traces extending alongside one another.

34. An assembly as claimed in claim 33 wherein said conductive features
of at least one said transmission line include three traces extending alongside
30 one another.

35. An assembly as claimed in claim 31 wherein said conductive features of at least some of said transmission lines include a signal trace and a first potential reference plane, said trace extending over said first potential reference plane, the dielectric element including dielectric material disposed
5 between said trace and said first potential reference plane.

36. An assembly as claimed in claim 35 wherein the conductive features on said dielectric element define a plurality of transmission lines as aforesaid,
10 said first potential reference plane being incorporated in a plurality of transmission lines and constituting the first reference element of each said transmission line.

37. An assembly as claimed in claim 33 or claim 34 or claim 35 or claim
15 36 wherein at least some of said transmission lines have adjacent-connected ends, the conductive features of the transmission line being connected to a multiply-connected element through a plurality of adjacent contacts on said chip at each such adjacent-connected end.

20 38. An assembly as claimed in claim 37 further comprising flexible leads connecting said conductive features on said dielectric elements to said contacts, said flexible leads at least some of said adjacent-connected ends including a set of plural separate flexible leads extending next to one another.

25 39. An assembly as claimed in claim 38 wherein the leads in each said set of plural flexible leads are curved and extend substantially parallel to one another.

40. An assembly as claimed in claim 37 further comprising flexible leads
30 connecting said conductive features on said dielectric elements to said

contacts, said flexible leads at least some of said adjacent-connected ends including a plural-conductor flexible lead incorporating a plurality of conductors extending next to one another and a dielectric between such conductors.

5

41. An assembly as claimed in claim 31 wherein said multiply-connected elements are operative to send and receive said signals to one another as digital signals through said transmission lines in synchronism with a common clock.

10

42. An assembly as claimed in claim 41 wherein said first chip includes an internal clock and said multiply-connected elements are operative to send and receive said digital signals in synchronism with said internal clock.

15

43. An assembly as claimed in claim 41 wherein said multiply-connected elements include a cache memory and a unit operative to read data from said cache memory, or to write data to said cache memory, or both.

20

44. An assembly as claimed in claim 31 wherein the conductive features on said dielectric element define a plurality of transmission lines as aforesaid, said first chip including an internal clock for generating clock signals and a plurality of clock-timed elements adapted to send and receive signals in synchronism with said clock signals, said internal clock being connected to said clock-timed elements by one or more of said transmission lines so that said clock signals can be transmitted to said clock-timed elements along the features of said sets.

25

45. An assembly as claimed in claim 31 wherein said dielectric element is movable with respect to said chip, the assembly further comprising

deformable conductive elements interconnecting said at least some of said contacts on said chip with said conductive features on said dielectric element.

46. An assembly as claimed in claim 45 further comprising a compliant material disposed between said chip and said dielectric element.

47. A method of making a semiconductor device comprising the steps of:

(a) providing a unitary semiconductor structure having a front surface, said semiconductor structure incorporating a plurality of electronic elements within said structure and contacts on said front surface, said electronic elements having signal connections, at least some of said signal connections being connected to said contacts;

(b) assembling a dielectric structure having a electrically conductive features thereon to said semiconductor structure so as to connect the electrically conductive features with said contacts through deformable conductive elements so that at least some signal connections of said electronic elements within said unitary semiconductor structure are connected to one another through said contacts, said deformable conductive elements and said conductive features on said dielectric structure, and so that said dielectric structure remains movable with respect to said semiconductor structure.

48. A method as claimed in claim 47 wherein said unitary semiconductor structure includes a plurality of chips, said assembling step being performed so that electronic elements within each said chip are connected to one another through conductive features within a portion of the dielectric structure associated with that chip, the method further comprising the step of severing said unitary semiconductor structure to separate each said chip from the unitary semiconductor structure so that the portion of the dielectric structure associated with such chip remains with the chip.

49. A method as claimed in claim 48 wherein said dielectric structure is a unitary dielectric structure incorporating a plurality of said portions, said severing step being performed so as to sever said dielectric structure.

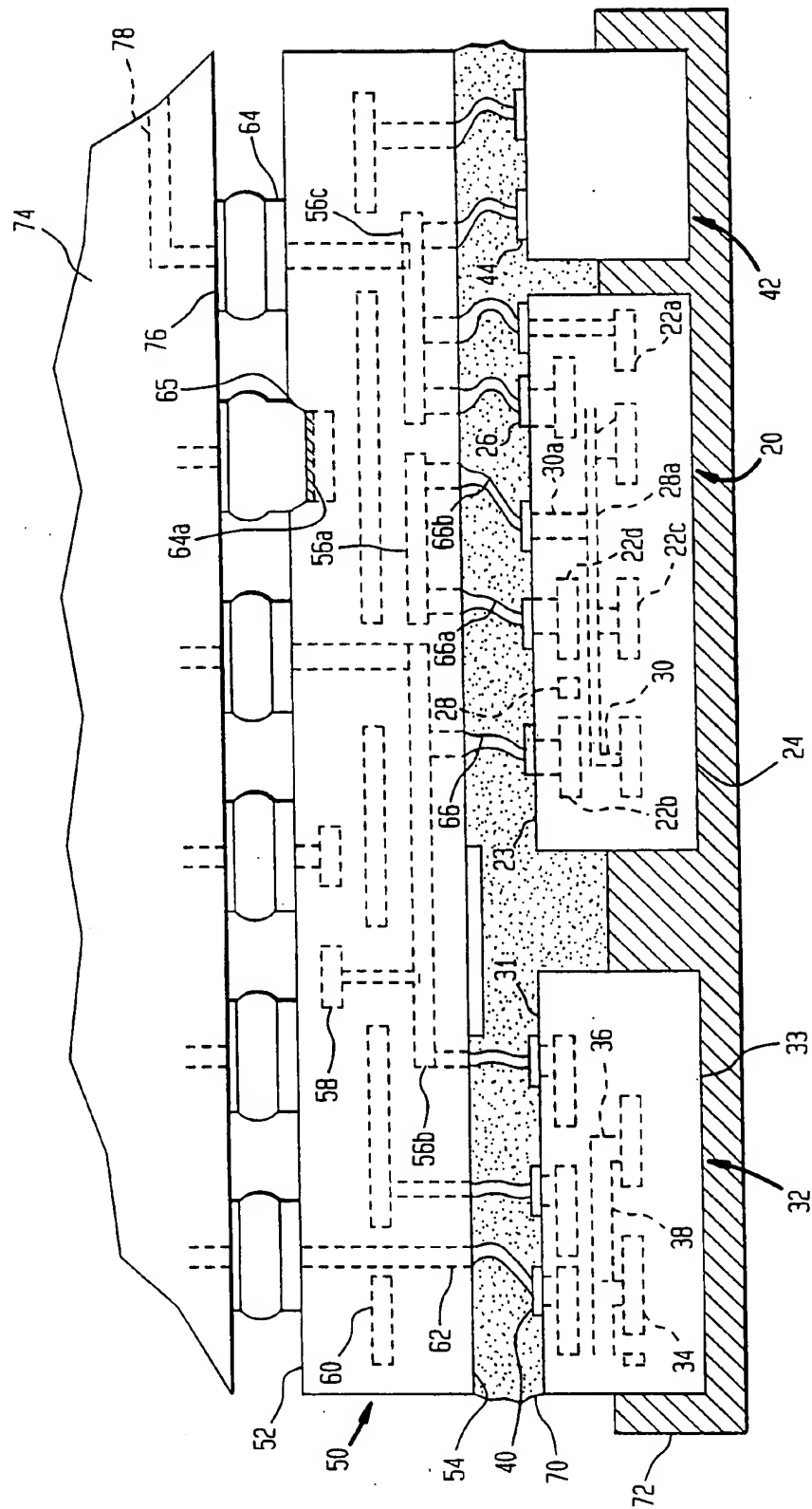
5 50. A method as claimed in claim 48 wherein said dielectric structure includes a plurality of separate components, said assembling step being performed so that one said component is assembled to each said chip.

10 51. A method as claimed in claim 47 wherein said deformable conductive elements include flexible leads, said assembling step including the step of deforming said flexible leads through a predetermined displacement.

52. A method as claimed in claim 47 further comprising the step of providing a compliant material between said dielectric element and said chip.

15

FIG. 1



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FIG. 2

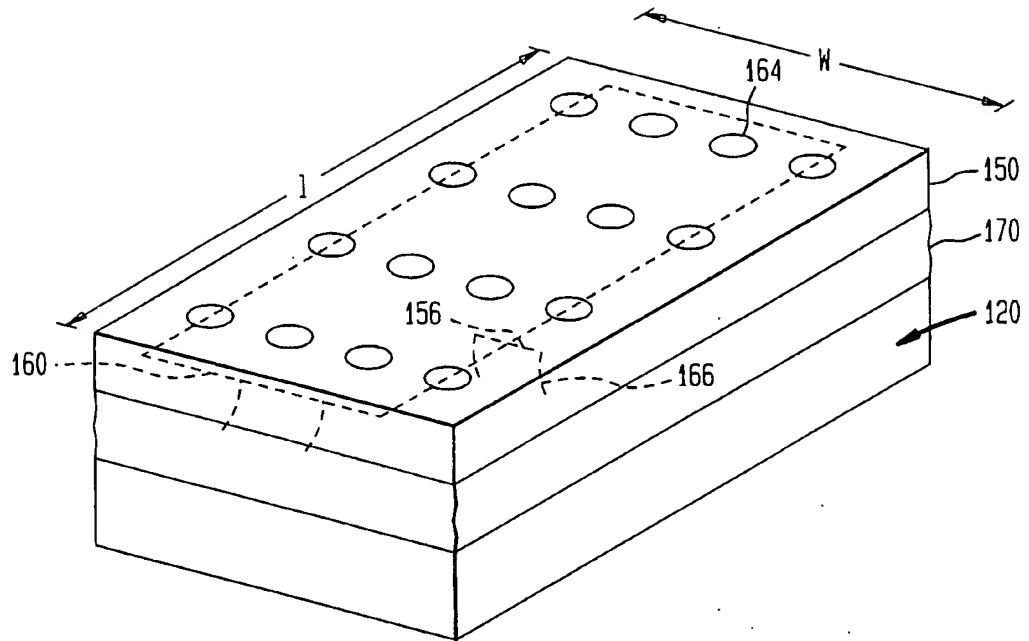
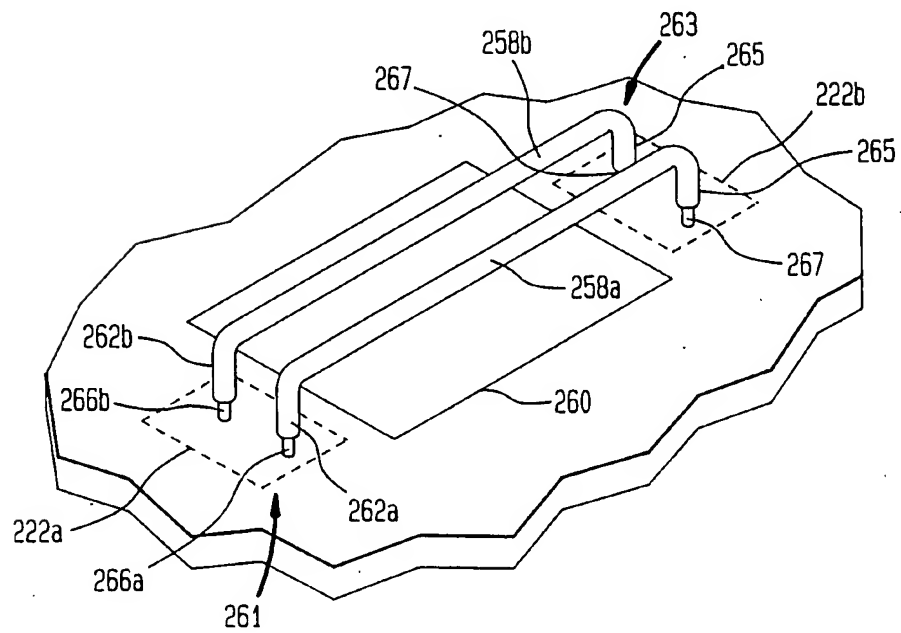


FIG. 3



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FIG. 4

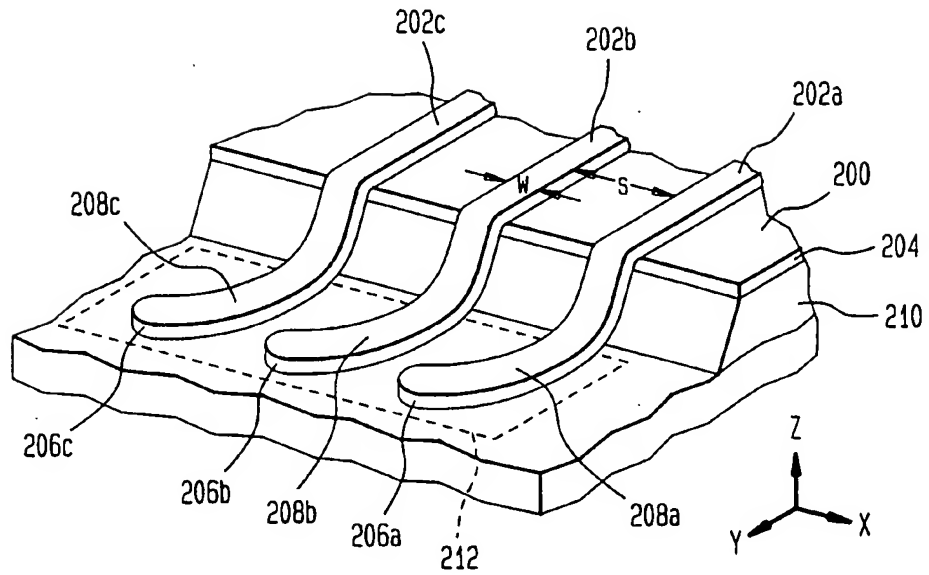
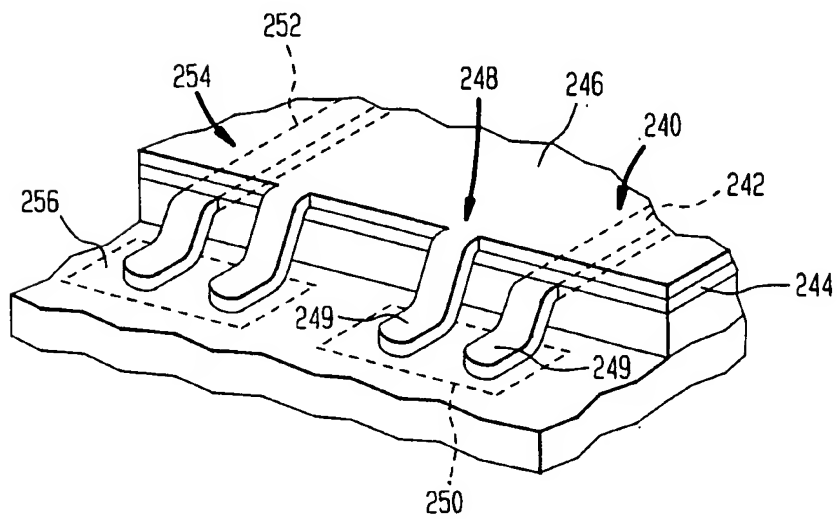


FIG. 5



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FIG. 6

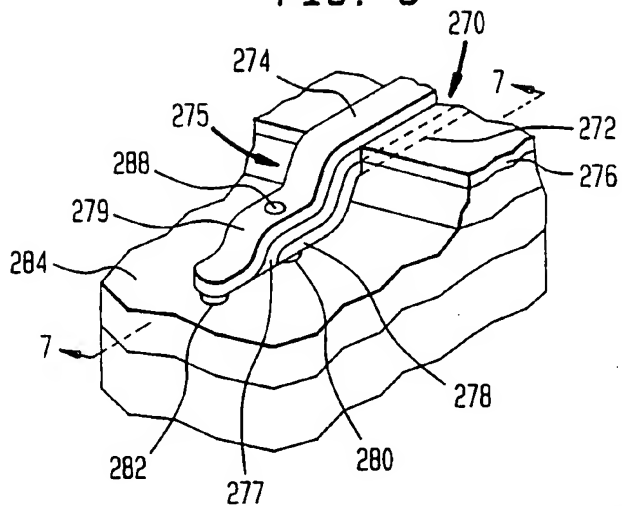


FIG. 7

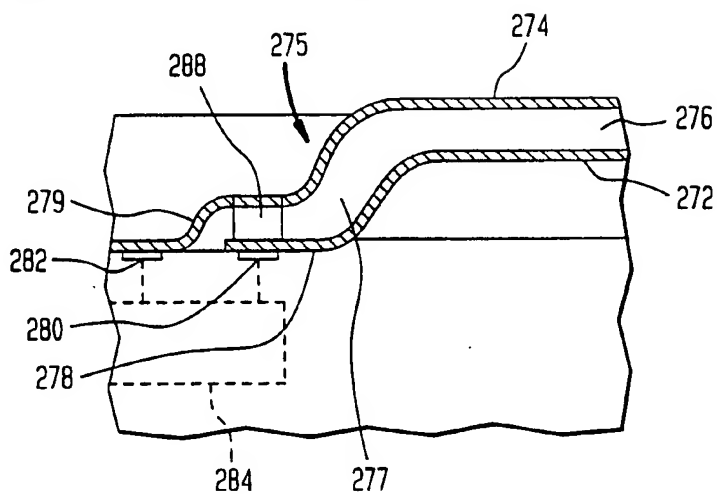


FIG. 8

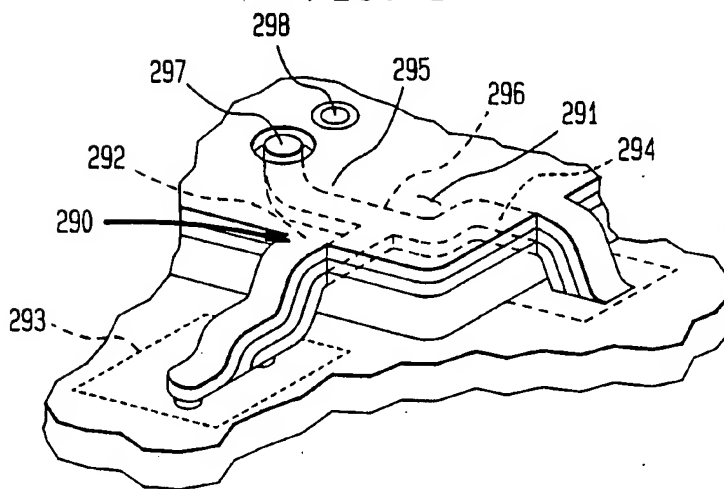
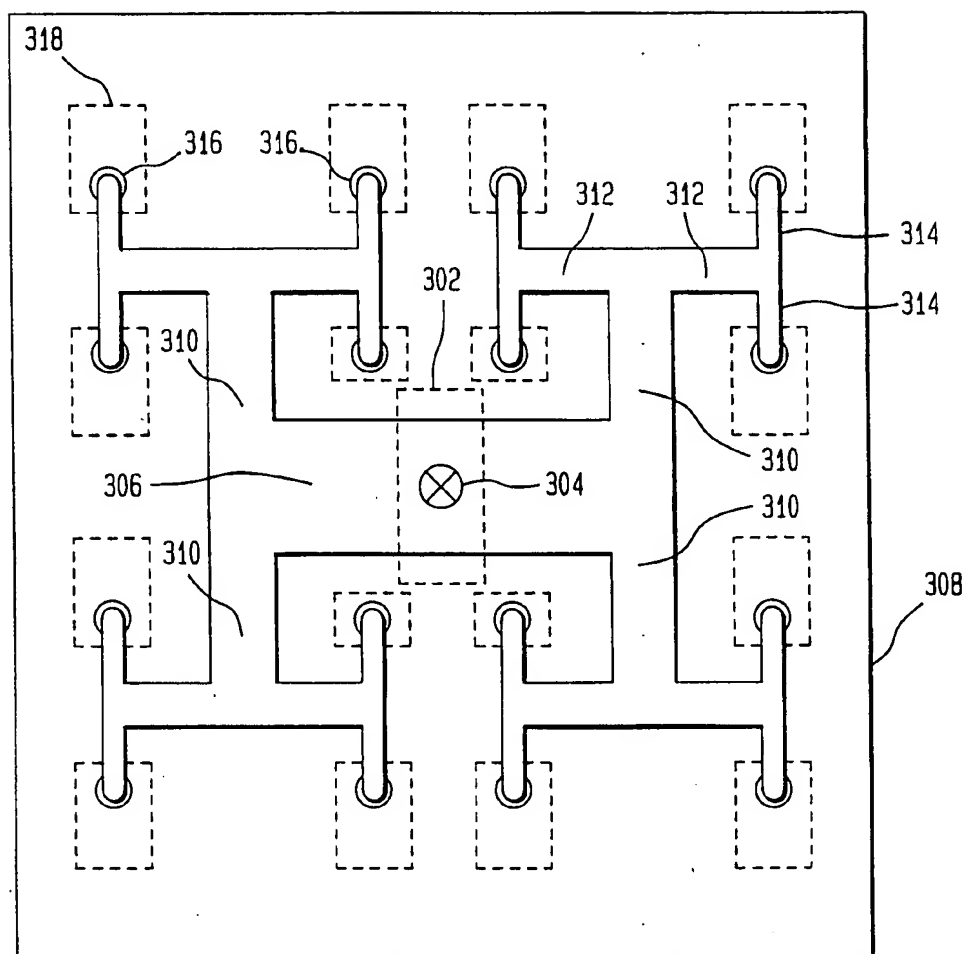
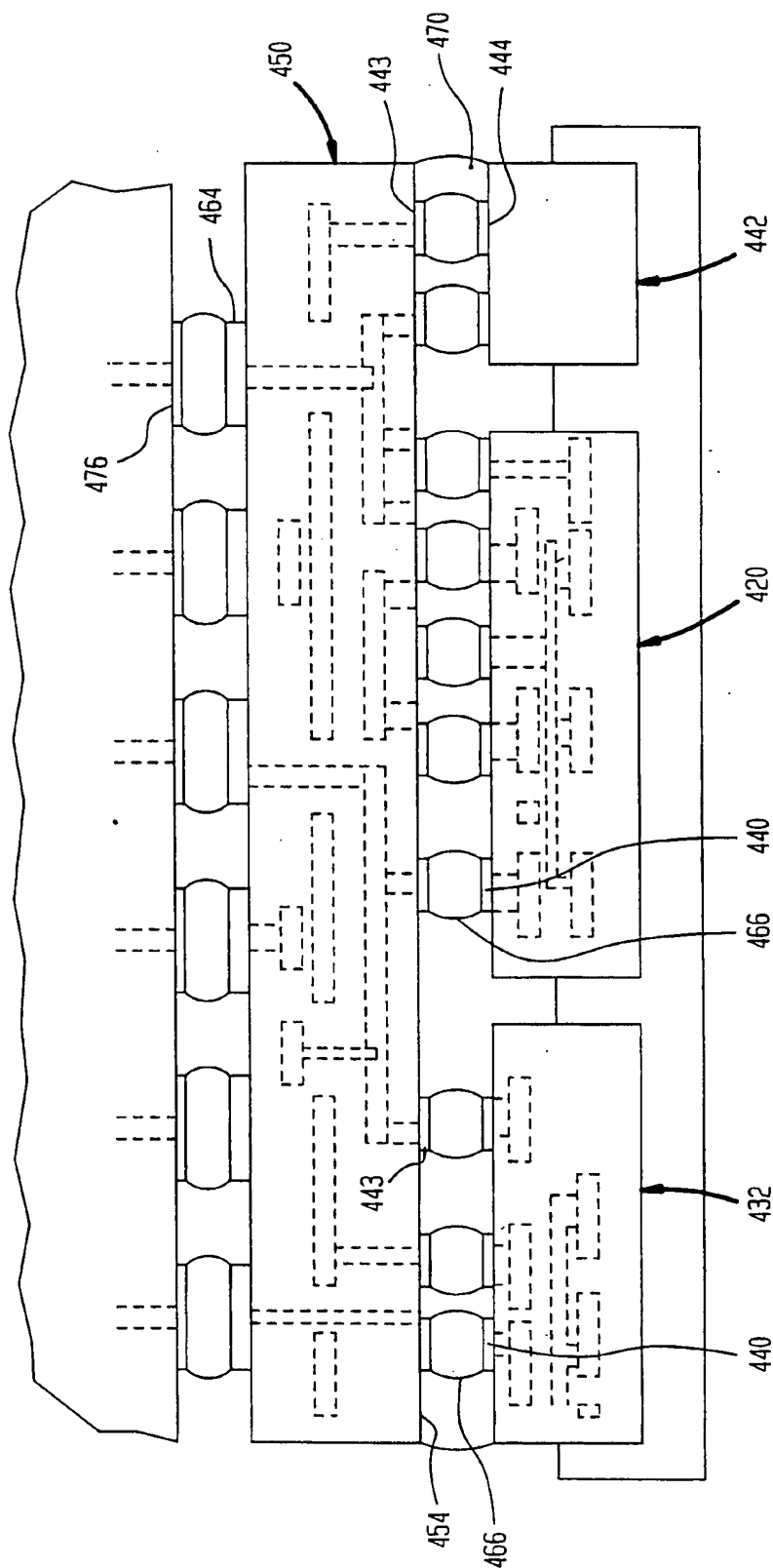


FIG. 9



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FIG. 10



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FIG. 11

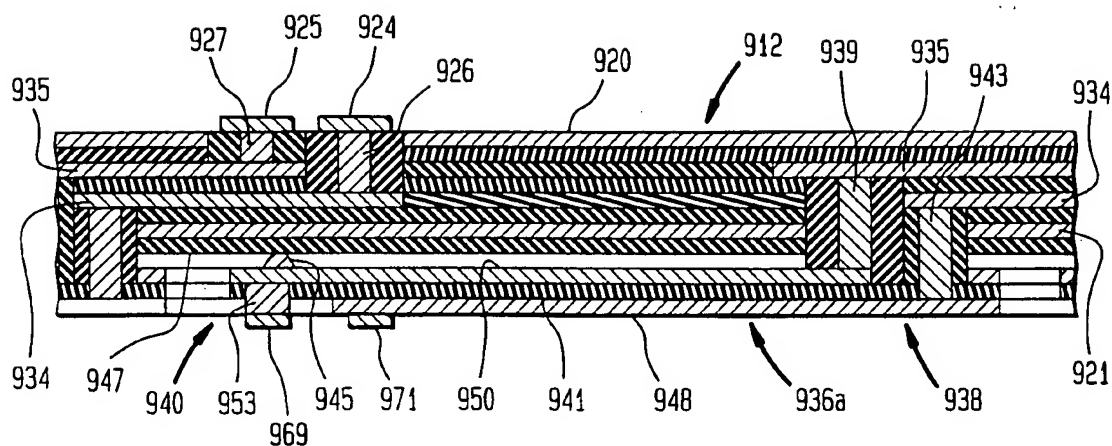
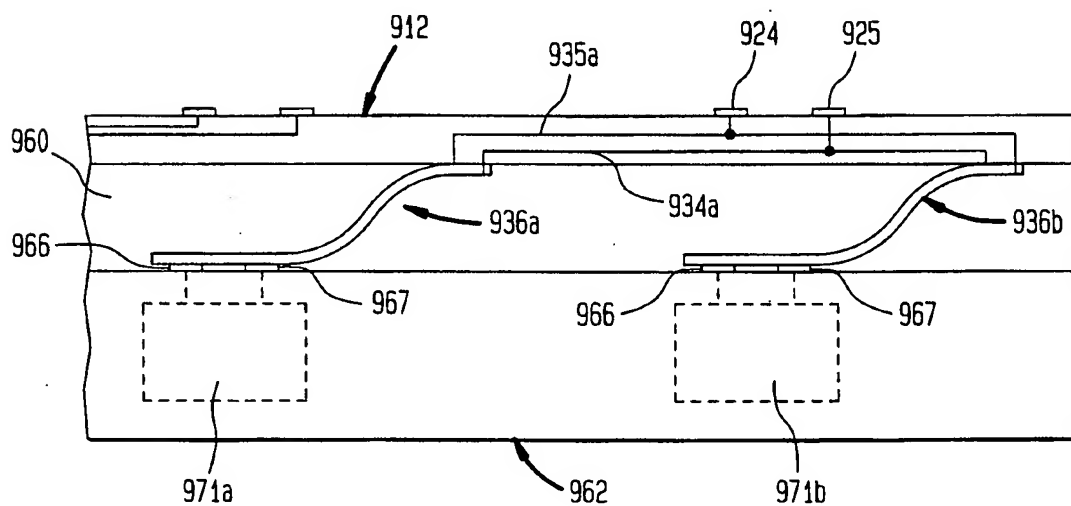


FIG. 12



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FIG. 13

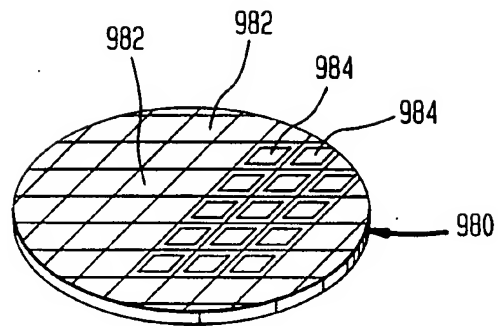
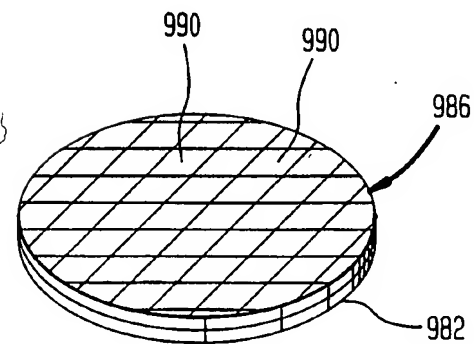


FIG. 14



INTERNATIONAL SEARCH REPORT

International application No.
PCT/US98/06486

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) : H01L 29/40, 23/34, 23/48, 23/52

US CL : 257/664, 725, 728, 778; 333/247

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 257/664, 725, 728, 778; 333/247

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
NONE

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
USPTO APS

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X --- Y	US 5,281,151 A (ARIMA ET AL) 25 January 1994 (25.01.94), col. 6, lines 32-43.	1-7, 11-21, 31-40, 45 ----- 8-10, 22-30, 41-44, 46-52
Y	US 4,021,838 A (WARWICK) 03 May 1977 (03.05.77), figure 2.	1-52
Y	US 5,212,403 A (NAKANISHI ET AL) 18 May 1993 (18.05.93), figure 1.	1-52
Y	US 5,510,758 A (FUJITA ET AL) 23 April 1996 (23.04.96), figure 14.	8-10, 46
Y	US 5,523,622 A (HARADA ET AL) 04 June 1996 (04.06.96), entire document.	1-52



Further documents are listed in the continuation of Box C.



See patent family annex.

*

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document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

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document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

A

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Date of the actual completion of the international search

04 JUNE 1998

Date of mailing of the international search report

10 AUG 1998

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